Integrated Circuit Design and
Implementation Courses

Supported by
Ministry of Foreign Affairs, ROC(Taiwan)

Taiwan-Europe Semiconductor Short-term Training Program 2026

Program 1
Jun 29- Jul 24

Design Trends and Technological Transformations in Semiconductor for 2 week: National Taiwan University

or Advanced Semiconductor Manufacturing and Process Integration for 2 week: National Cheng Kung University
&
Pratical Training for 2 weeks:
Taiwan Semiconductor Research Institution

Program 2
Jul 13- Jul 24

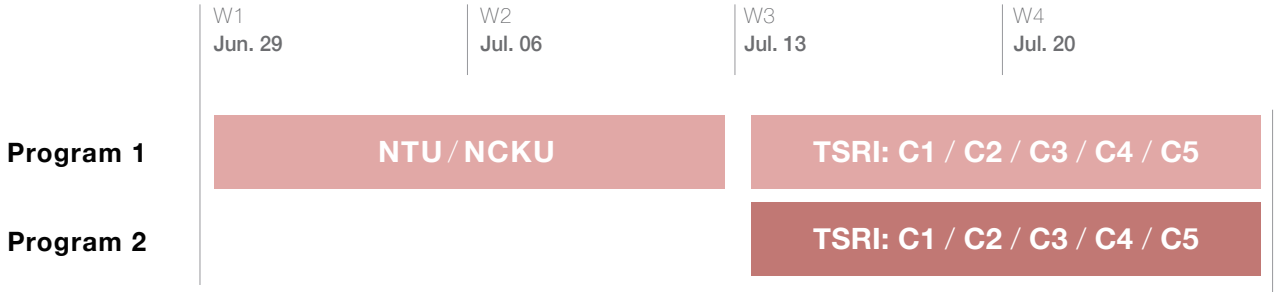
Pratical Training for 2 weeks:
Taiwan Semiconductor Research Institution

July, 2026

Program Introduction

This summer, we are offering two 4-week training programs to choose from.
The first program runs from June 29 to July 24, starting with two weeks of classes at either National Taiwan University (NTU) or National Cheng Kung University (NCKU), followed by two weeks of hands-on training at TSRI.
The second program runs from July 13 to July 24 and will be conducted entirely at TSRI.

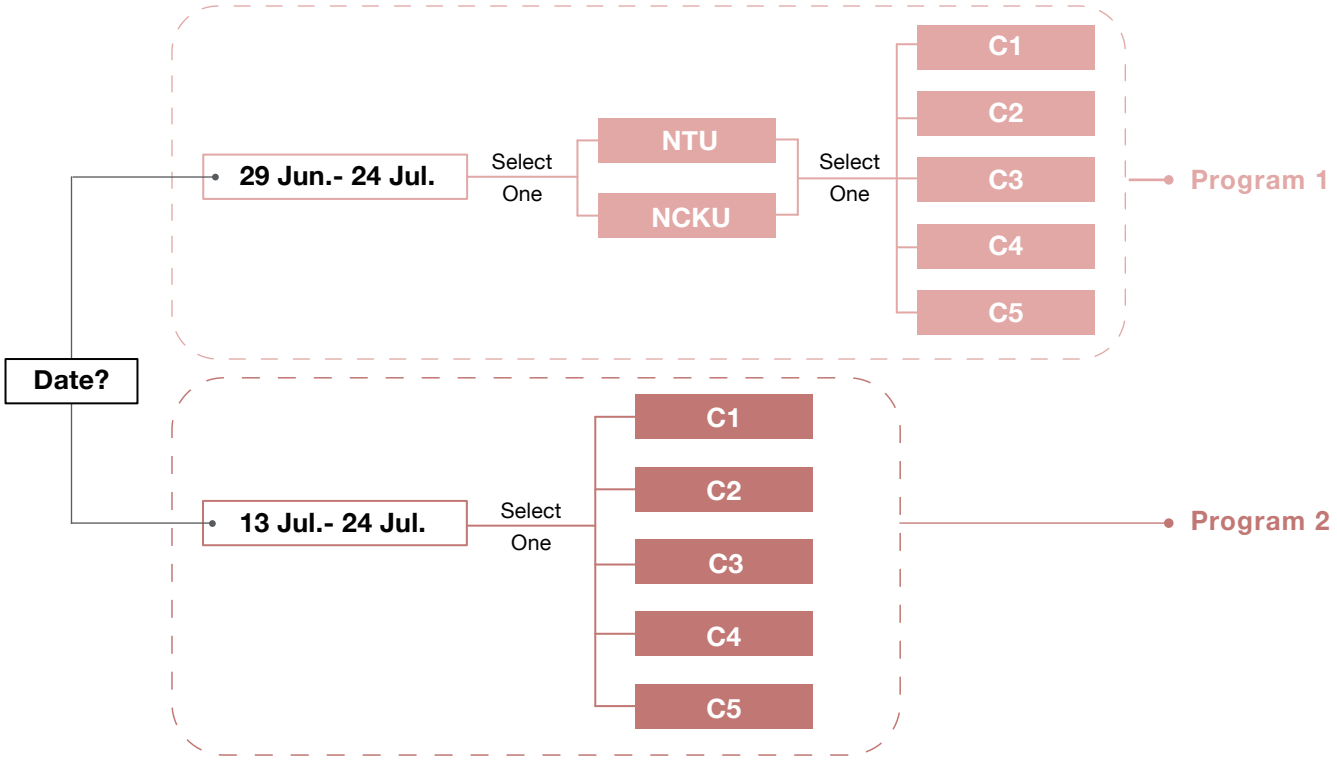
Program Timeline



C1 CMOS MEMS IC Design and Simulation
C2 Silicon Photonics and PIC Design
C3 Practical Amplifier and Power Management IC Design（TSRI, Tainan）
C4 Advanced Packaging Technologies & Practice（TSRI, Tainan）
C5 AI/IoT SoC FPGA Prototyping

How to Enroll?

Each course has a limited number of spots available. Please register early to secure your place.
The organizer reserves the right of final decision.



NTU

2026 Taiwan-Europe Semiconductor Short-term Training Program

Design Trends and Technological Transformations in Semiconductor

** Schedule is subject to change

NTU Courses

	Morning Session	Afternoon Session
JUN 29	- Orientation/ Campus Tour - Welcome Lunch	Introduction of Semiconductor in Taiwan
JUN 30	The History and Future of Chip Design and Manufacturing (Chip Wars)	- Silicon photonics
JUL 01	IC Technologies	- IC Technologies - Project Discussion
JUL 02	Semiconductor Devices and Physics	- Semiconductor Devices and Physics - Project Discussion
JUL 03	One Day Trip Culture Visit	
JUL 06	Analog Integrated Circuit Design	NTU NEMS Research Center/ Project Discussion
JUL 07	Electronic Design Automation	NTU NEMS Research Center/ Project Discussion
JUL 08	Digital Integrated Circuit Design	Computational and AI for Next-Generation Semiconductor Materials
JUL 09	Industry Visit Science Park Exploration Museum	TSMC Museum
JUL 10	- Final Presentation - Farewell Lunch	Discovery Taiwan
JUL 11	Check-out and Departure to TSRI	

NCKU

2026 Taiwan-Europe Semiconductor Short-term Training Program

Advanced Semiconductor Manufacturing and Process Integration

** Schedule is subject to change

NCKU Courses – 2 Credits

	Morning Session	Afternoon Session
JUN 29	11:10 Opening Ceremony	Introduction to ULSI and Semiconductor Device Physics
JUN 30	NCKU Campus Tour & National Museum of Modern Art Tainan	CMOS Process Integration and Process Flow
JUL 01	Introduction to Lithography and Light Engineering	- National Museum of Taiwan History - Our Land Our People: The Story of Taiwan
JUL 02	Lithography Systems and EUV Technology	Process Modules I: Thermal Processes
JUL 03	Process Modules II: Ion Implantation	Chinese Language Course- Pronunciation & Characters
JUL 06	Heterogeneous Integration and Industry-Academia Collaborative Research	Process Modules III: Wet and Dry Etching Technologies
JUL 07	Process Modules IV: Thin-Film Deposition and Dielectrics	Chinese Language Course- Introductions & Communication
JUL 08	Process Modules V: Metallization and Interconnect Technology	Chinese Language Course-Food & Daily Expressions
JUL 09	Process Modules VI: Chemical Mechanical Polishing (CMP)	Chinese Language Course-Everyday Tasks
JUL 10	Advanced CMOS Devices and Process Control	Chinese Language Course-Transport & Culture
JUL 11	- Hotel Check-out - 10:10 Group Presentation & Closing Ceremony	Departure to TSRI

TSRI

Overall of Courses in TSRI

C1 CMOS MEMS IC Design and Simulation

Target Audience:

Undergraduate students (junior year or above) and graduate students (master's and PhD) in electronics, electrical engineering, mechanical engineering, or related disciplines with an interest in MEMS. Priority will be given to applicants with VLSI or MEMS coursework (grade A- or higher) or related research experience.

Courses Schedule

Jul 13

- Preview of MEMS Technology
- TSRI CMOS MEMS Process
- Lab: Accelerometer Layout Design (Simulation Version)

Jul 14

- Applications of CMOS MEMS Technology
- Characterizing the MEMS Devices
- Lab: Accelerometer Layout Design (Tape-out Version)

Jul 15

- Applications of Accelerometer
- Design and Architecture of Accelerometer
- Simulation by CoventorWare

Jul 16

- TSRI CMOS MEMS Process Flow and Design Rules
- TSRI CMOS MEMS MPW
- The MEMS Measuring Instruments in TSRI
- Visit to the MEMS Measurement Laboratory

Jul 17

- Circuit Design Flow: From Simulation to Verification
- Introduction of Capacitive Sensing Readout Circuit、IP User Guide
- Lab: G-sensor readout circuit simulation and integrate MEMS with readout circuit

Jul 20

- Application and Working Principle of Resonator
- Design and Architecture of Resonator
- Lab: Resonator Simulation and Layout Design (Simulation Version)

Jul 21

- Lab: Resonator Layout Design (Tape-out Version)
- Introduction and Design of TIA Readout Circuit
- Lab: Simulation of TIA Circuit(Pre-sim)

Jul 22

Industry Visit

Jul 23

- TIA Layout Guideline/Layout Verification
- Lab: Lab: Simulation of TIA Circuit(Post-sim)

Jul 24

- Lab: Combined MEMS and Readout Circuit Simulation and Layout
- MEMS Measurement Laboratory Hands-on Operation

TSRI

Overall of Courses in TSRI

C2 Silicon Photonics and PIC Design

Target Audience:

This course is open to undergraduate and graduate students from departments such as Electrical Engineering, Electronics, Photonics, Physics, Chemistry, or other related disciplines. Applicants should have a minimum academic performance of A- (or equivalent) or above in their relevant coursework.

Courses Schedule

Jul 13
- Overview of Silicon Photonics Processes

Jul 14
- Silicon Photonics Process Technology
- MPW Tape-Out Flow

Jul 15
- System Requirements of PIC Systems
- End-to-End PIC Design Flow

Jul 16
- Design Environment Setup
- Schematic Entry

Jul 17
- Simulation Methodology
- OptSim Simulations

Jul 20
- PIC Layout Design Fundamentals
- Basic Layout Design

Jul 21
- Schematic Driven Layout (SDL)
- Hands-on Exercise 1 (Generate PIC layout from schematic)

Jul 22
- Industry Visit

Jul 23
- Hands-on Exercise 2 (PIC Layout Design for Driver/TIA/Ser-Des Co-Integration)
- Hands-on Exercise 3 (Electrical-optical interface layout)

Jul 24
- Hands-on Exercise 4 (DRC Debugging and Full-Clean Layout for Photonic Devices)
- Closing Ceremony (Afternoon)

TSRI

Overall of Courses in TSRI

C3 Practical Amplifier and Power Management IC Design (TSRI, Tainan)

Target Audience:

This course is open to undergraduate and graduate students who have Fundamental knowledge of Electronics (semiconductor devices and circuit analysis) and Hands-on experiences with the Full-Custom VLSI design flow, including circuit design and layout using Cadence Virtuoso, and physical verification via Mentor Calibre.

Courses Schedule

Jul 13

Practical OPAMP Design-Process & OPAMP Introduction

Jul 14

- Practical OPAMP Design-Single-Stage OPAMP Design
- Practical OPAMP Design-gm/id lab

Jul 15

- Practical OPAMP Design-Single-Stage OPAMP Design
- Practical OPAMP Design-gm/id lab

Jul 16

- Practical OPAMP Design-opamp/bias design lab
- Practical OPAMP Design-two-stage OPAMP Design

Jul 17

- Practical OPAMP Design-two-stage OPAMP Design
- Practical OPAMP Design-Miller-Compensated opamp design lab

Jul 20

Practical Power Management IC Design-Introduction of BCD Process

Jul 21

Practical Power Management IC Design-High Voltage Circuit Design

Jul 22

Practical Power Management IC Design-Protection Mechanisms in BCD Process

Jul 23

Practical Power Management IC Design-Protection Mechanisms in BCD Process

Jul 24

Closing Ceremony

TSRI

Overall of Courses in TSRI

C4 Advanced Packaging Technologies & Practice (TSRI, Tainan)

Target Audience:

This course is open to undergraduate and graduate students who have Fundamental knowledge of semiconductor devices, manufacturing and physics.

Courses Schedule

Jul 13	Jul 14	Jul 15	Jul 16	Jul 17
- Orientation & Safety - Facility	- Introduction to Semiconductor Manufacturing - SPC & Process Monitoring	- Lithography Process - Etching Process	- Thin Film Deposition - Wafer Thinning	Laboratory Visit and Equipment Orientation
Jul 20	**Jul 21**	**Jul 22**	**Jul 23**	**Jul 24**
- Lithography Process_Practice - Etching Process_Practice(1)	- Thin Film Deposition(1) - Etching Process_Practice(2)	- Thin Film Deposition(2) - Introductory Wafer Thinning and CMP Training	- Introduction to Wafer Dicing Process - Bonding Process	Closing Ceremony

TSRI

Overall of Courses in TSRI

C5 AI/IoT SoC FPGA Prototyping

Target Audience:

Undergraduate (junior or above), master's, and PhD students in electronics, electrical engineering, or EECS-related fields, with strong interests in Digital or SoC IC design. Priority given to those who have completed IC/System design-related course with a grade of A- or above)

Prerequisites:

Prerequisite theory courses are Logic Design and VLSI Design, with fundamental concepts of digital circuit design. Understanding of Verilog Hardware Description Language (mandatory requirement), as well as basic syntax of C and Python languages. Understanding of SoC design concepts and basic Linux operation skills are preferred.

Courses Schedule

Jul 13	Jul 14	Jul 15	Jul 16	Jul 17
Arm Cortex-M55 IoT SoC Platform tutorial	H/W FPGA Prototyping	Firmware development	Adding an AI Accelerator IP to SoC Platform	Industry Visit

Jul 20	Jul 21	Jul 22	Jul 23	Jul24
Arm Cortex-A55 AI SoC Platform tutorial	SoC FPGA Prototyping (Hardware)	SoC FPGA Prototyping (Firmware)	SoC FPGA Prototyping (Application)	Closing Ceremony

July, 2026

Information

Participant Support

- Each participant will receive a daily allowance of NTD 1,000.
- The round-trip tickets for participants will be arranged by the relevant Taiwan Representative Office.
- Accommodation in Taiwan will be arranged by the host organization.

Requirements

- A scanned copy of a passport valid for at least six months.
- Digital passport-size color photos taken within the past six months.
- A scanned copy of the official transcripts for each academic year.
- Other supporting documents (e.g., English proficiency certificate, transcript showing completion of a VLSI Design course with a grade of A- or above)

Contact Information

Please refer to the contact details of the training organizers and the seven Taiwan Representative Offices in Europe below.

Training Organizers

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02 **NCKU's Academy of Innovative Semiconductor and Sustainable Manufacturing**

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03 **Taiwan Semiconductor Research Institute**

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Taiwan Representative Offices In Europe

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